Pipeline Stage Unification for Low-Power Consumption

Department of Information Electronics
Graduate School of Engineering
Nagoya University

Hajime Shimada, Hideki Ando,
Toshio Shimada

Outline

- Background
  - Demands for low-power processors
  - Low-power consumption with Variable Supply Voltage (VSV)
  - Limitations of VSV in future technology
- Proposal
  - Pipeline Stage Unification (PSU) for low-power consumption
- Evaluation
  - Energy reduction
- Conclusions

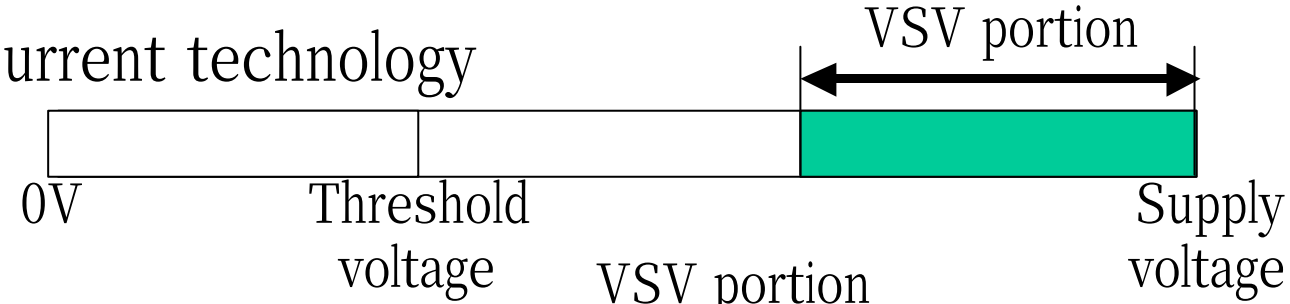
Demands for Low-Power Processors

- Needs for low-power processors
  - Mobile computers
  - Embedded systems
- Reasons for low-power
  - For long battery life
  - For easy thermal design

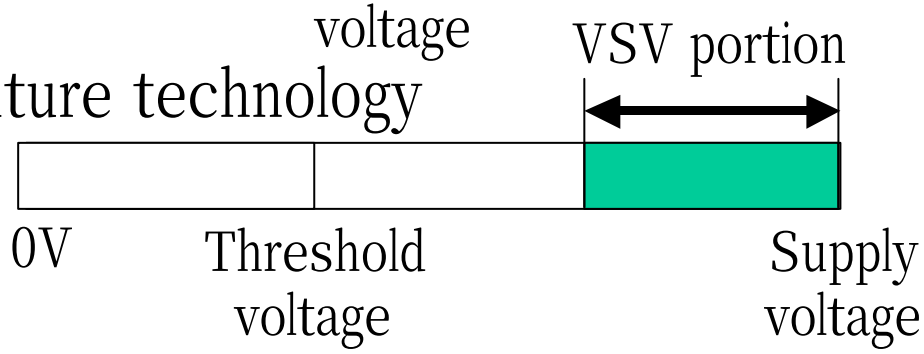
Both high-performance and
low-power are demanded

Low-Power Consumption with Variable Supply Voltage (VSV)

- Recent mobile processors use Variable Supply Voltage (VSV)
  - Transmeta Crusoe
  - Intel XScale
- Limitations of VSV
  - Current technology



  - Future technology



Pipeline Stage Unification (PSU) for Low-Power Consumption

- Most of current processors have a deep pipeline
  - To achieve high clock frequency
  - It divides traditional one stage to multiple stages

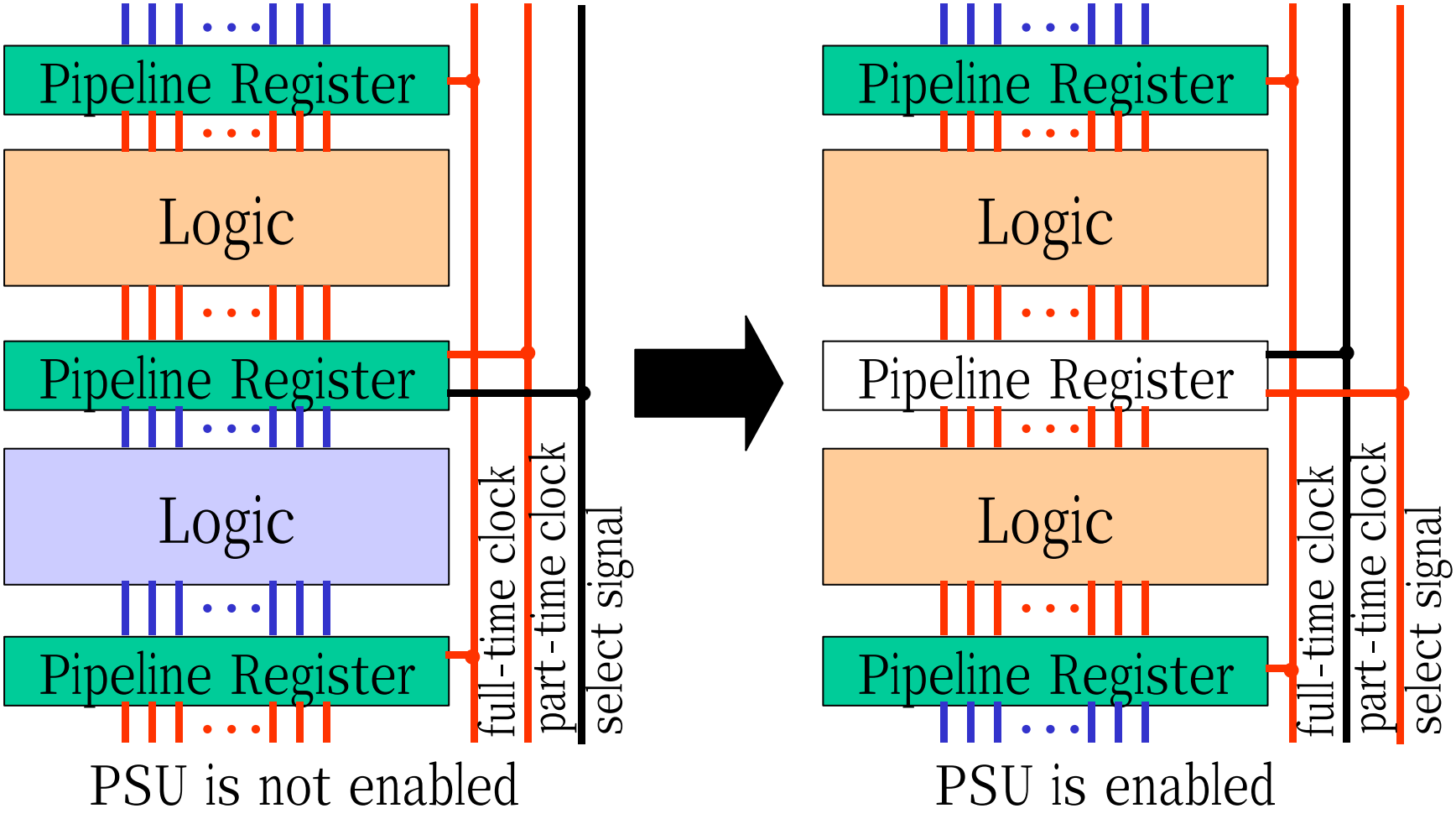
- When a processor runs at low clock frequency mode
  - Deep pipeline is not needed
  - Deep pipeline is harmful for instruction throughput

We propose Pipeline Stage Unification (PSU) when processor runs at low-clock frequency mode

Advantages of PSU

- Increase of instruction throughput by reducing several latencies
  - Unification of fetch, decode, register read and issue stages
    →Reduction of branch misprediction penalty
  - Unification of cache access stages
    →Reduction of cache hit latencies
- Reduction of power consumption
  - When PSU is enabled, pipeline registers between unified stages are stopped
    →Number of transistors which clock drives are reduced
    →Power consumption of clock driver is reduced

Implementation of PSU



Estimation of Power Reduction

- We refer to the power consumption data of Compaq Alpha 21264
- Clock driver of Alpha 21264 consumes 32% of power [Gowan98]
- We assumed that power is reduced in proportion to the activity reduction of pipeline registers
  - Two stages are united: 16% is reduced
  - Four stages are united: 24% is reduced

Simulation Environment

- Simulator: SimpleScalar tool set
- Instruction set: SimpleScalar PISA
  (based on MIPS R10000)
- Benchmarks: 8 programs from SPECint95
- We evaluated execution time with various pipeline stages
  - Evaluation of energy

    $$\text{Energy} = \text{Power} \times \text{Execution time}$$

Processor Configuration

- 8-issue superscalar processor
- 64 entry instruction window
- Branch predictor
  - 8K entry gshare and 2K entry BTB
- Cache
  - 64KB L1 instruction/data and 2MB L2 unified
- Variations of latencies

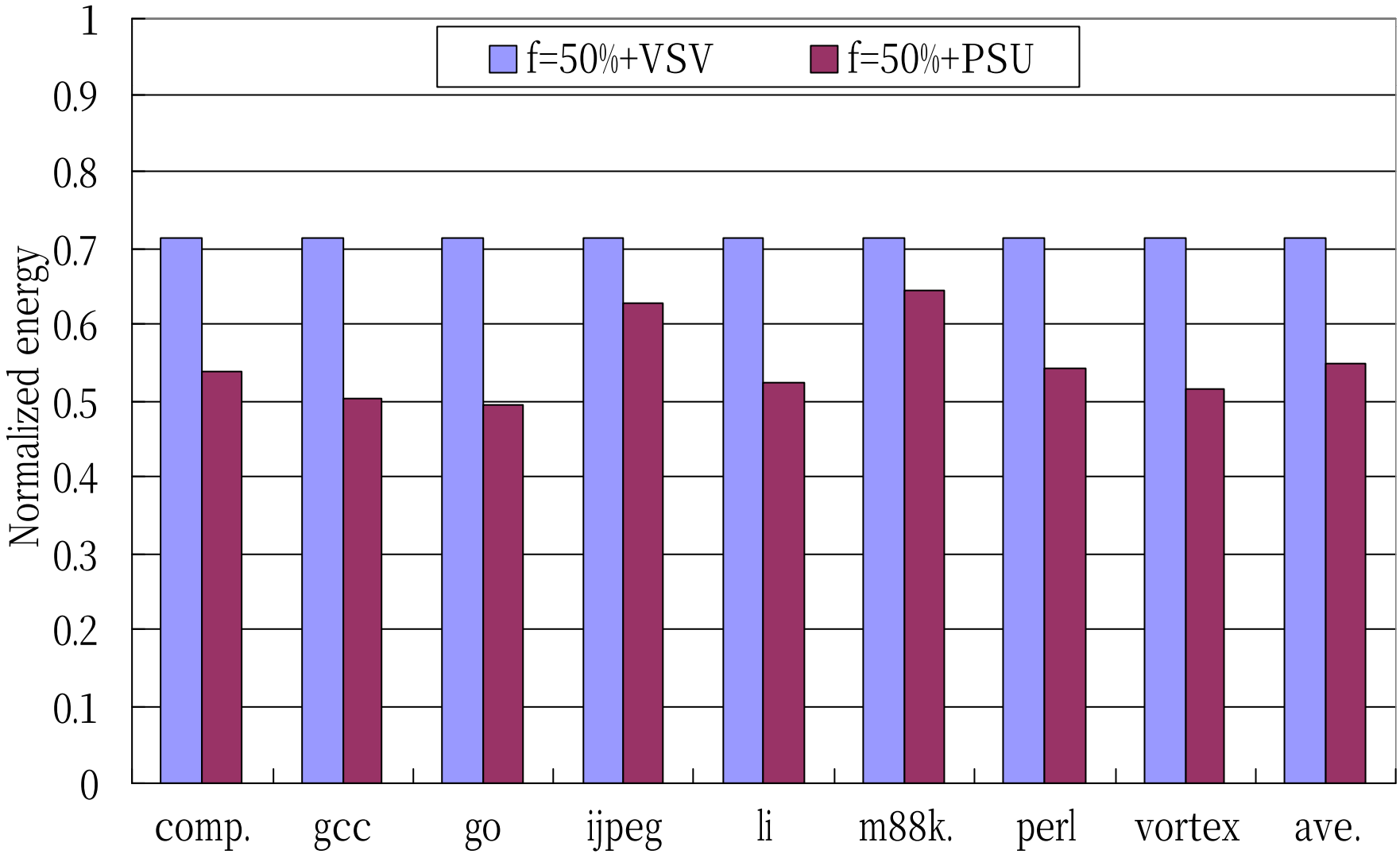
Clock frequency(f)	100%	50%	25%
Branch misprediction penalty	20	10	5
L1 cache hit latency	4	2	1
L2 cache hit latency	16	8	4

Assumption of Energy Estimation

Assumed relationship of clock frequency and supply voltage derived from Crusoe TM5400

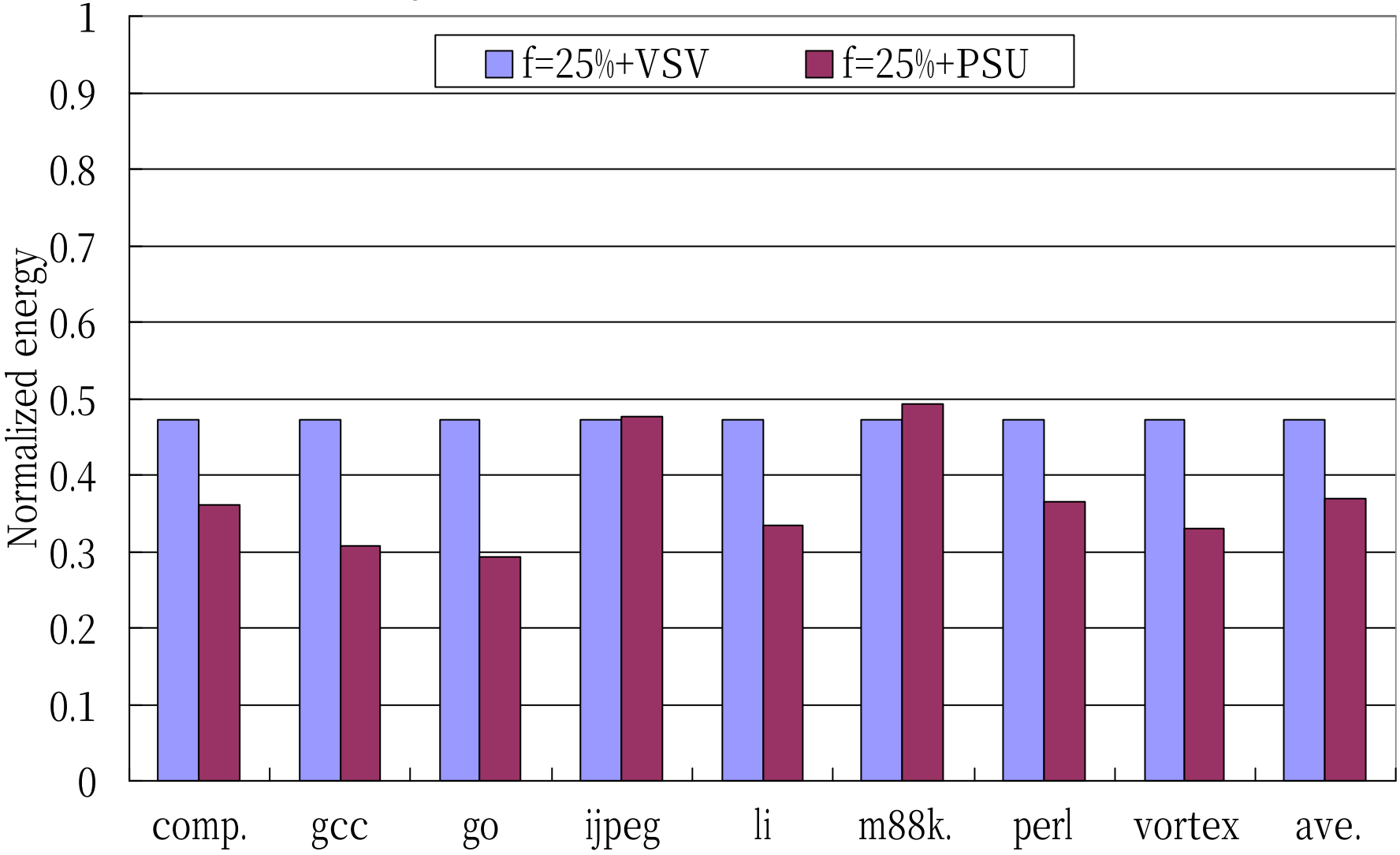
- With VSV
  - Assumed VSV of TM5400
    - f=100%: Supply voltage 1.60V
    - f=50%: Supply voltage 1.35V
    - f=25%: Supply voltage 1.10V
- With PSU
  - Assumed default supply voltage of TM5400
    - f=100,50,25%: Supply voltage 1.60V

Energy Reduction in f=50%



Energy consumption is improved by 23% in f=50%

Energy Reduction in f=25%



Energy consumption is improved by 21% in f=25%

Conclusions

- Conclusions
  - We proposed PSU for low-power consumption
  - Energy reduction is improved from VSV
    - Improved by 23% in f=50% and 21% in f=25%
  - VSV is inefficient in future technology

    →Improvement of energy reduction will increase