VI. Conclusion

This paper quantified the issue queue delay, and showed the delay for various queue sizes. Our evaluation results are useful as a quick reference in microarchitectural design. In the evaluation, we designed the banked tag RAM, and identified the correct critical path of the issue queue. With these optimizations, the issue queue delay is reduced by up to 20% in the sizes we explored, compared with a simple design with a monolithic tag RAM and simple calculation of the delay.

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